Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of the Claims:

1-16 (Cancelled)

17. (New) A method comprising:

dispatching a predicate instruction for execution before a predicate of the predicate instruction is resolved;

dispatching subsequent instructions for execution before the predicate is resolved; and

stalling dispatch of a consumer instruction of the predicate instruction if the predicate remains unresolved.

18. (New) The method of claim 17 further comprising executing the predicate instruction and storing a result of the executed predicate instruction in a buffer in a writeback path if the predicate of the predicate instruction is unresolved.

19. (New) The method of claim 18 further comprising:

resolving the predicate;

writing the result to an architectural register file if the predicate has a predicate value of true, and discarding the result if the predicate value is false; and

updating a scoreboard with a resolved status for the predicated instruction.

20. (New) The method of claim 17 further comprising dispatching the consumer instruction when the predicate of the predicate instruction is resolved.

21. (New) The method of claim 20 further comprising checking a scoreboard to determine if the predicate of the predicate instruction is resolved.

22. (New) An apparatus comprising:

means for dispatching a predicate instruction for execution before a predicate of the predicate instruction is resolved;

means for dispatching subsequent instructions for execution before the predicate is resolved; and

means for stalling dispatch of a consumer instruction of the predicate instruction if the predicate remains unresolved.

23. (New) The apparatus of claim 22 further comprising means for executing the predicate instruction and storing a result of the executed predicate instruction in a buffer in a writeback path if the predicate of the predicate instruction is unresolved.

24. (New) The apparatus of claim 23 further comprising:

means for resolving the predicate;

means for writing the result to an architectural register file if the predicate has a predicate value of true, and discarding the result if the predicate value is false; and

means for updating a scoreboard with a resolved status for the predicated instruction.

25. (New) The apparatus of claim 22 further comprising means for dispatching the consumer instruction when the predicate of the predicate instruction is resolved.

26. (New) The apparatus of claim 25 further comprising means for checking a scoreboard to determine if the predicate of the predicate instruction is resolved.

27. (New) An apparatus comprising:

an instruction pipeline with a plurality of pipeline stages wherein:

a predicate instruction is dispatched for execution within the pipeline before a predicate of the predicate instruction is resolved;

subsequent instructions are dispatched for execution within the pipeline before the predicate is resolved; and

a consumer instruction of the predicate instruction is stalled from dispatching if the predicate remains unresolved;

a register file coupled to the pipeline;

a buffer coupled to the register file and coupled to a writeback stage of the pipeline, the buffer to store predicate instructions that have been executed and contain an unresolved predicate;

a scoreboard coupled to the register file, the scoreboard to track the status of instructions within the pipeline;

28. (New) The apparatus of claim 27 wherein the buffer is an associative buffer coupled to a writeback path of the processor.

29. (New) The apparatus of claim 27 wherein the buffer is a reorder buffer.

30. (New) The apparatus of claim 27 wherein the status of instructions within the pipeline includes the resolved status of predicates for predicated instructions.

31. (New) An apparatus comprising an instruction pipeline with a plurality of pipeline stages wherein:

a predicate instruction is dispatched for execution within the pipeline before a predicate of the predicate instruction is resolved;

subsequent instructions are dispatched for execution within the pipeline before the predicate is resolved; and

a consumer instruction of the predicate instruction is stalled from dispatching if the predicate remains unresolved.

32. (New) A system comprising:

a processor, the processor to

dispatch a predicate instruction for execution before a predicate of the predicate instruction is resolved;

dispatch subsequent instructions for execution before the predicate is resolved; and

stall dispatch of a consumer instruction of the predicate instruction if the predicate remains unresolved; and

one of an audio input device or an audio output device coupled to the processor.

33. (New) The system of claim 32, wherein the processor comprises a scoreboard, the scoreboard to track the status of instructions within the processor.

34. (New) The system of claim 32, wherein the processor comprises a buffer, the buffer to store predicate instructions that have been executed and contain an unresolved predicate